Integrating Cycle-Accurate Chisel Models with gem5's System Simulation

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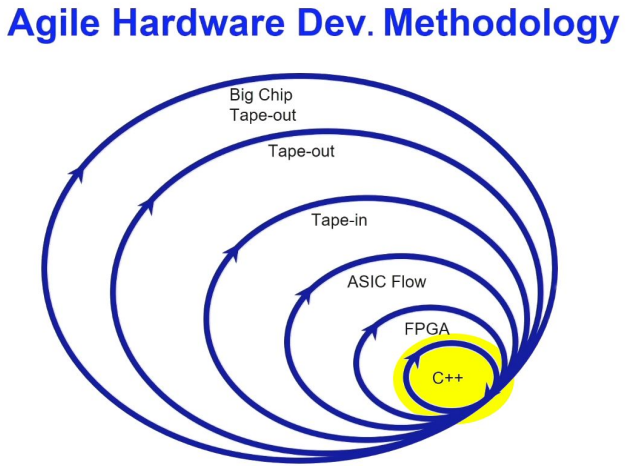
Selective Accuracy For Faster Iteration

- gem5 is a cycle-level simulator
  - Uses event driven model to simulate cycles
  - BUT does not necessarily represent actual hardware implementation
  - High Level Emulation (HLE)

- Need Cycle Accurate simulator
  - C++ model generated from verilog by verilator
  - Accurately models hardware components for each clock cycle
  - Low Level Emulation (LLE)

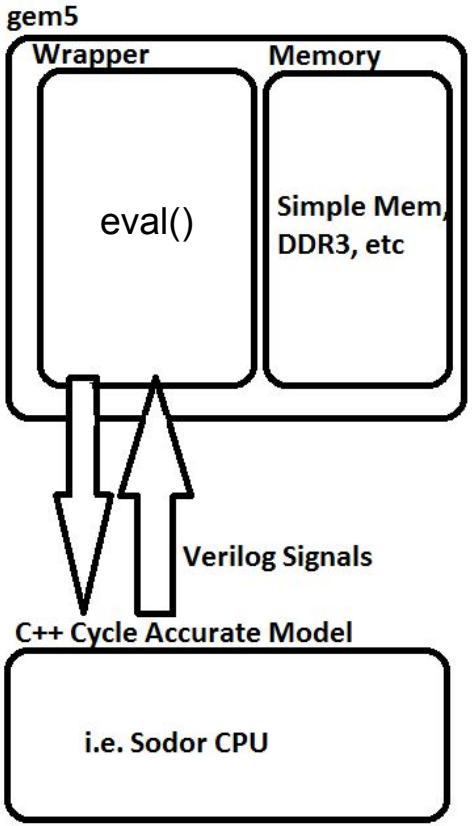


From Hennessy and Patterson Turing Lecture

Integrating The Models

- Verilator Wrapper
  - Uses Verilator generated code
  - Set verilog signals in C++ model

- Write Wrapper For Any Component
  - Chisel and Verilog BlackBox for HLE targets
  - Gem5 Wrapper for LLE targets



Future work & questions for you

- Can we use FIRRTL to simulate?
- Other ideas and models to integrate
- How would **you** use cycle accurate gem5?