TOWARD RETHINKING THE MANAGEMENT TECHNIQUES IN EMERGING MEMORY SYSTEMS

Maryam Babaie, Ayaz Akram, Jason Lowe-Power
DArchR Research Group, CS Department, University of California Davis
{mbabaie, yazakram, jlowepower}@ucdavis.edu

CWIDCA Workshop at MICRO-55
Chicago, IL, USA
Oct. 2022
Motivation

HPC systems rely on heterogeneous memory, e.g., Knights Landing, Cascade Lake, Sapphire Rapids.

We need to rethink memory management.

😢 No accurate model available for community.

We extend gem5\(^1\) with a heterogeneous/disaggregated memory system model for design space exploration of future HPC systems. We add support for:

1. DRAM Cache  
2. HBM interface and controller  
3. Modular memory controller design

---

gem5’s DRAM Cache Support

A. Dedicated DRAM Cache Controller
   1. Unified DRAM Cache & Memory Controller
   2. Disaggregated DRAM Cache Controller

B. Decoupled DRAM Cache Policy Manager
   • Supports multiple cache architectures in parallel

Goal: Enabling cycle-level analysis of DRAM cache designs for data management research
gem5’s DRAM Cache Validation

Performance Validation
1. Read bandwidth compares well with the theoretical peak.
2. Access amplification is same as in real hardware\(^1\).

Functional Validation
• Successfully tested Linux kernel booting
• Tested GAPBS and NPB benchmark suites

\(^1\) M. Hildebrand, J. T. Angeles, J. Lowe-Power, and V. Akella, “A case against hardware managed dram caches for nvrram based systems,” in 2021 ISPASS.
Thank you and see you in the poster session 😊

Questions:
Maryam Babaie
mbabaie@ucdavis.edu