Potential and Limitation of High-Frequency Cores and Caches

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***Abstract*—This paper explores the potential of cryogenic computing and superconducting electronics as promising alternatives to traditional semiconductor devices. As semiconductor devices face challenges such as increased leakage currents and reduced performance at higher temperatures, these novel technologies offer high performance and low power computation. Cryogenic computing operates at ultra-low temperatures near 77 K, leading to lower leakage currents and improved electron mobility. On the other hand, superconducting electronics, operating near 0 K, allow electrons to flow without resistance, offering the potential for ultra-low-power, high-speed computation. This study presents a comprehensive performance modeling and analysis of these technologies and provides insights into their potential benefits and limitations. We implement models of in-order and out-of-order cores operating at high clock frequencies associated with superconducting electronics and cryogenic computing in gem5. We evaluate the performance of these components using workloads representative of real-world applications like NPB, SPEC CPU2006, and GAPBS. Our results show the potential speedups achievable by these components and the limitations posed by cache bandwidth. This work provides valuable insights into the performance implications and design trade-offs associated with cryogenic and superconducting technologies, laying the foundation for future research in this field using gem5. Our code and data are open-source and available on GitHub[1].**

I. Introduction

Traditional semiconductor devices suffer from increased leakage currents and reduced performance as temperatures rise [1], leading to significant energy dissipation and limiting the scalability of modern computing systems. Coupling this with a slowing Moore's Law [2], the performance improvements of traditional computing systems have stagnated. As a countermeasure, researchers are exploring novel computing technologies which promise high performance and low power computation.

Cryogenic computing, operating at ultra-low temperatures near 77 K, presents a promising avenue on high-speed and low-power computation [1]. Another technology, superconducting electronics, operating at near 0 K, offers the potential for ultra-low-power, high-speed computation, by allowing electrons to flow without resistance [3]. These technologies allow for individual components to operate at a higher clock frequency than typical CMOS devices.

[1]https://github.com/darchr/gem5-cryo-superconducting

In this paper, we study the full-system implications of running the processing core at ultra-high frequencies. Specifically, we introduce a modeling framework and perform and initial evaluation of out-of-order and in-order cores at high clock frequencies associated with superconducting electronics and cryogenic computing. We also wish to substantiate how these speedups will affect other components in the system, and how these other components should be designed to keep up with the faster components.

To evaluate the performance of cryogenic and superconducting computing technologies, we:

1) Use gem5 [4], [5] to implement models of in-order and out-of-order cores operating at high clock frequencies, typical of cryogenic and superconducting environments.
2) Choose workloads representative of real-world applications like NPB [6], SPEC CPU2006 [7], and GAPBS [8] to evaluate the performance of these components. These workloads provide a comprehensive understanding of how different types of applications respond to the ultra-fast processing capabilities offered by cryogenic and superconducting technologies.
3) Simulate these workloads in different combinations of the aforementioned components in a superconducting clock domain and in the cryogenic clock domain, while keeping the board and memory at their room temperature frequencies.
4) Show the potential speedups we can get from the combinations along with the potential limitation posed by the cache bandwidth required for that speedup.

II. Background

In recent years, the pursuit of novel computing paradigms has led to a resurgence of interest in cryogenic components and superconducting circuits. These technologies promise unprecedented speedups by exploiting the unique properties of materials at extremely low temperatures.

While superconducting was first discovered in 1911 [9], the theoretical concepts behind it were not fully understood until the BCS theory of the 1950s [10]. Due to further work in concepts like the Josephson effect [11] and flux quantization [12], superconducting circuits have been understood to operate at high clock frequencies of up to 100 GHz [13]. Therefore, superconducting circuits enable ultra-fast signal processing with minimal energy dissipation [3].

Cryogenic components offer improved performance and energy efficiency by the reduced resistance at ultra-low temperatures. At cryogenic temperatures, semiconductor devices exhibit lower leakage currents and improved electron mobility, leading to improved performance. Therefore, cryogenic components also operate at a higher clock frequency, usually around 4 GHz [1].

Cryogenic computing has gained significant attention in recent years, with researchers exploring cryogenic components to enhance computing performance. Byun et al. introduced CryoCore, a cryogenic core based on the BOOM core, operating at 4.0 GHz with improved performance at cryogenic temperatures [1]. Min et al. proposed CryoCache, a cryogenic cache hierarchy leveraging these temperatures to enhance cache performance [14]. These components operate at ultra-low temperatures and offer substantial speedups compared to conventional semiconductor devices.

Our work represents a crucial step towards the practical implementation of superconducting and cryogenic components in computing systems. Notably, we:

1) Demonstrate the feasibility of integrating high-level characteristics of these components into gem5 [4], [5].
2) Show the potential speedups and limitations of high-frequency components, providing valuable insights into the performance implications and design trade-offs associated with these novel technologies.
3) Lay the foundation for gem5 as a modeling framework for this field of computing research, providing all the tools necessary for evaluating the performance of computing systems under cryogenic and superconducting conditions.

III. Methodology

For all the experiments, we used gem5 [4], [5] as the simulator. We leverage the easy modification of gem5 CPU and cache models to make our own custom components, which is essential due to the microarchitectural details of the cryogenic computing models available in the literature. We can also place the CPU, caches, and memory in different clock domains, which is essential for simulating cryogenic computing environments. The gem5 Resources artifacts [15] provides workloads that we can also use for our experiments. Hence, gem5 is the ideal choice for our experiments.

A. Core Microarchitecture

We modeled the cryogenic core and caches by building a model based on CryoCore by Byun et al. [1]. Their cryogenic core was based on BOOM [16], an out-of-order RISC-V core, and could run at 4.0 GHz. We used microarchitectural details provided in their paper to create a variant of the O3CPU in gem5. These microarchitectural details are enumerated in Table I. For the pipeline values that were not specified, we went with the default values provided by gem5 for those variables. With regard to the latencies of the functional units and the branch predictor, we decided to go with the ones provided as part of the *RISCVMatched* prebuilt board [17] (based on the HiFive Unmatched and having a similar architecture to Rocket and BOOM [18]), since these values have been partially validated [19].

We also created an in-order variant of the CryoCore, called the In-Order CryoCore, which is based on the pre-built *RISCV-Matched* board [17] in gem5. This core is based on the HiFive Unmatched core, which is an in-order core. The pipeline comprises of eight stages: two stages of instruction fetch (F1 and F2), two stages of instruction decode (D1 and D2), address generation (AG), two stages of data memory access (M1 and M2), and register write-back (WB) [20]. Execution takes place either in the AG stage or the M2 stage, depending on the instruction. This core has been partially validated [19].

The latencies of the functional units and the branch predictor for both the CryoCore and the In-Order CryoCore are the same as the ones provided in the *RISCVMatched* board [17]. These values can be viewed in Table II.

TABLE I: Microarchitectural details of the gem5 model of CryoCore[2]

Parameter	Value in gem5 Model
Cache Load/Store Ports	1
Instruction Width	4 bytes
Fetch Queue Size	24
Load/Store Queue Entries	24
Instruction Queue Entries	72
Reorder Buffer Entries	96
Integer Registers	180
Floating Point Registers	168

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TABLE II: Common microarchitectural details of the gem5 model of CryoCore and In-Order CryoCore[3]

Parameter	Value in gem5 Model
BTB Entries	32
RAS Entries	12
Branch Predictor Size	16 KB
History Table Size	4 KB
Indirect Branch Predictor Size	16 entries
Branch Predictor Counter Bits	4
Integer FU Latency	1
Multiplication FU Latency	3
Division FU Latency	6
Memory Read/Write Latency	2

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B. Cache Microarchitecture

We modelled the cache hierarchy based on CryoCache by Min et al. [14]. Their design has a private L1 cache, a private L2 cache, and a shared L3 cache. We used microarchitectural details provided in their paper to create a variant of the cache hierarchy in gem5 with those details. They can be viewed in greater detail in Table III.

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[2]Found in components/cryocore/cryocore.py
[3]Found in components/cryocore/cryocore.py
[4]Found in components/cryocache/cryocache.py

TABLE III: Microarchitectural details of the gem5 model of CryoCache[4]

Parameter	Value in gem5 Model
L1D Cache Size	32 kB
L1D Cache Associativity	8
L1D Cache Data Latency	2
L1I Cache Size	32 kB
L1I Cache Associativity	8
L1I Cache Data Latency	2
L2 Cache Size	512 kB
L2 Cache Associativity	8
L2 Cache Data Latency	8
L3 Cache Size	16 MB
L3 Cache Associativity	16
L3 Cache Data Latency	21

C. Workloads

For the workloads, we used a combination of small and large-sized benchmarks that are representative of real-world applications. The small-sized workloads are provided as part of the "`riscv-getting-started-benchmark-suite`" [21] suite provided as part of gem5 Resources. This suite's constituent workloads have been cherry-picked from popular benchmarks and applications. These workloads are as follows:

- `bfs` - Breadth First Search from the GAP benchmark suite [8]. We used a graph with 1024 vertices and 10 iterations.
- `tc` - Triangle Counting from the GAP benchmark suite [8]. We used a graph with 1024 vertices and 10 iterations.
- `minisat` - A SAT solver from the LLVM test suite [22]. We used a SAT problem of 15000 variables and 20000 clauses.
- `is` - Integer Sort from the NAS Parallel Benchmarks [6]. We used the class S version of this workload.
- `lu` - Lower-Upper Gauss-Seidel from the NAS Parallel Benchmarks [6]. We used the class S version of this workload.
- `cg` - Conjugate Gradient from the NAS Parallel Benchmarks [6]. We used the class S version of this workload.
- `bt` - Block Tri-Diagonal from the NAS Parallel Benchmarks [6]. We used the class S version of this workload.
- `ft` - Fourier Transform from the NAS Parallel Benchmarks [6]. We used the class S version of this workload.

For the large workloads, we used a subset of the SPEC CPU2006 [7] benchmark suite, that is compatible with the RISC-V ISA in gem5. These workloads are:

- `400.perlbench` - A Perl interpreter.
- `401.bzip2` - A file compression utility.
- `410.bwaves` - A fluid dynamics simulation.
- `429.mcf` - A vehicle scheduling problem.
- `433.milc` - A lattice quantum chromodynamics simulation.
- `434.zeusmp` - A computational fluid dynamics simulation.
- `435.gromacs` - A molecular dynamics simulation.
- `437.leslie3d` - A fluid dynamics simulation.
- `444.namd` - A molecular dynamics simulation.
- `445.gobmk` - A game of Go AI.
- `456.hmmer` - A bioinformatics program.
- `458.sjeng` - A chess program.
- `459.GemsFDTD` - A finite-difference time-domain method simulation.
- `462.libquantum` - A quantum computer simulator.
- `464.h264ref` - An H.264 video encoder.
- `470.lbm` - A lattice Boltzmann method fluid dynamics simulation.
- `471.omnetpp` - A discrete event network simulator.
- `473.astar` - A pathfinding program.

The large workloads are computationally expensive, with complete executions taking months in gem5. Therefore, to reduce simulation time, we used the SimPoints technique [23] to identify representative regions of the workloads, and used their weights to compute how the entire workload would perform.

D. Experimental Setup

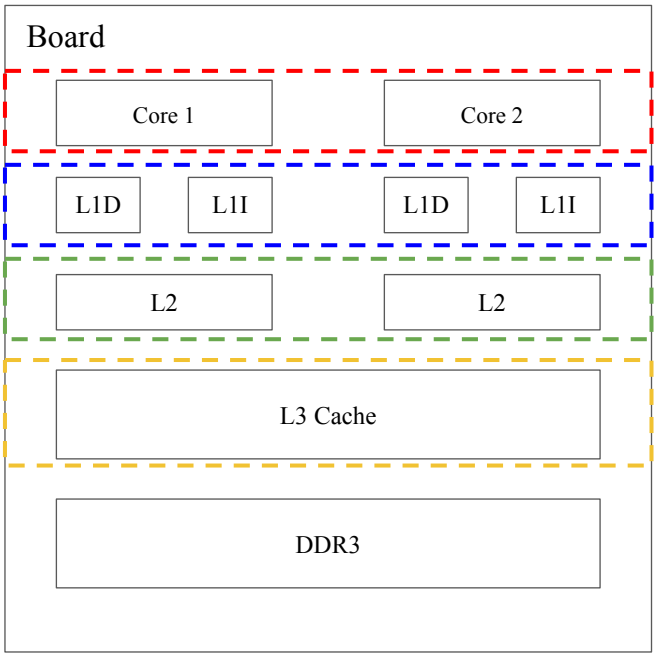


Fig. 1: Schematic representation of different clock domains of the board. Different colored rectangles represent different clock domains.

The experimental setup utilized a RISC-V system, or a "board", equipped with two CryoCores, each paired with a CryoCache. The memory system was comprised of a single-channel DDR3_1600_8x8-based DIMM.

We categorized the board's subcomponents into distinct clock domains, as illustrated in Figure 1. Specifically, the CryoCore, L1 Caches, L2 Caches, and L3 Cache are segregated into different clock domains. However, in all the experiments, the board itself operated at a constant room temperature clock

frequency of 2 GHz, while the memory system maintained its own constant frequency of 800 MHz.

We conducted a series of experiments to evaluate the performance of the workloads under varying clock frequencies. We varied the clock frequency of the CryoCore and the CryoCache in different combinations to observe the impact on the performance of the workloads. These configurations are as follows:

- *CryoCore and CryoCache (CryoAll)* - Out-of-order CryoCore and CryoCache models in the cryogenic clock domain (4 GHz).
- *SuperCore and CryoCache (SuperCryo)* - CryoCore model in the superconducting clock domain (100 GHz) and CryoCache model in the cryogenic clock domain (4 GHz).
- *SuperCore and SuperCache (SuperAll)* - CryoCore and CryoCache models in the superconducting clock domain (100 GHz).
- *In-Order CryoCore and CryoCache (In-Order CryoAll)* - In-order CryoCore model and CryoCache model in the cryogenic clock domain (4 GHz).
- *In-Order SuperCore and CryoCache (In-Order SuperCryo)* - In-order CryoCore model in the superconducting clock domain (100 GHz) and CryoCache model in the cryogenic clock domain (4 GHz).
- *In-Order SuperCore and SuperCache (In-Order SuperAll)* - In-order CryoCore and CryoCache models in the superconducting clock domain (100 GHz).

IV. Results

Our experimental setup allowed us to answer the following research questions:

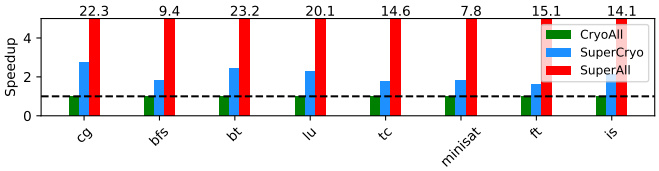
Research Questions

1) How does the performance of workloads vary with increasing clock frequency when subsystems are placed in a superconducting environment?
2) How is the performance of workloads affected by whether the core is out-of-order or in-order?
3) What new constraints must subsystems meet to leverage the improved performance resulting from increased clock frequency in a superconducting environment?

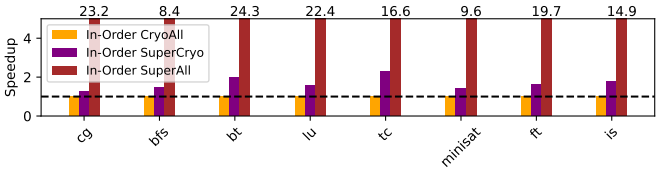
A. Workload Performance with Increasing Clock Frequency in Superconducting Environments

Figure 2a and 2b show the speedup of the small workloads with respect to the out-of-order and in-order cores. Specifically, it compares the speedups achieved by placing the core and/or cache in a superconducting environment, for both out-of-order and in-order cores.

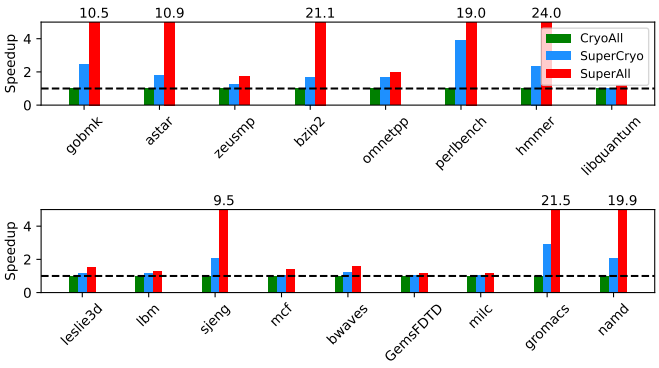
At a high level, the takeaways from these results are that placing both core and cache in a superconducting environment significantly boosts performance, and that speedups of in-order superconducting components over their cryogenic counterparts



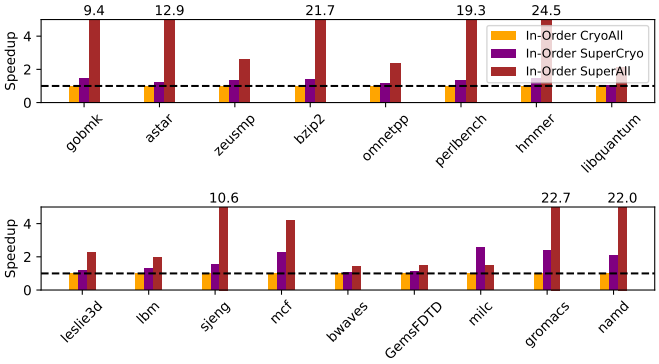
(a) Speedup of small workloads with respect to the out-of-order CryoCore and CryoCache configuration, in different out-of-order setups.



(b) Speedup of small workloads with respect to the in-order CryoCore and CryoCache configuration, in different in-order setups.



(c) Speedup of large workloads with respect to the out-of-order CryoCore and CryoCache configuration, in different out-of-order setups.



(d) Speedup of large workloads with respect to the in-order CryoCore and CryoCache configuration, in different in-order setups.

Fig. 2: Speedup of workloads with respect to their respective core architectures.

are generally higher than the speedups of out-of-order superconducting components over their cryogenic counterparts. By characterizing the workloads that benefit the most from superconducting components, we also provide insights into the design trade-offs associated with these novel technologies.

For out-of-order cores, Figure 2a shows the speedup of the

small workloads in various out-of-order core configurations, with respect to the out-of-order CryoCore and CryoCache configuration. The bars represent different configurations for different small workloads. If only the core is placed in the superconducting environment, the performance improvement is not substantial, with the maximum speedup for small workloads being 2.7× for the `cg` workload over the baseline for an out-of-order core. Overall, the speedups for the small workloads range from 1.8× to 2.7× for the out-of-order SuperCore and CryoCache configuration, compared to the out-of-order CryoCore and CryoCache configuration. If both the core and the cache are placed in the superconducting environment, the performance improvement is more substantial for the out-of-order core. The maximum speedup for the small workloads for an out-of-order SuperCore and SuperCache configuration is 23.2× for the `bt` workload over the baseline out-of-order CryoCore and CryoCache configuration. Some workloads like `lu` and `cg` also receive speedups of more than 20× for the out-of-order SuperCore and SuperCache configuration, compared to the out-of-order CryoCore and CryoCache configuration. However, some workloads like `bfs` and `minisat` do not receive substantial speedups, with the speedup being around 9.4× and 7.8× for the out-of-order SuperCore and SuperCache configuration, compared to the out-of-order CryoCore and CryoCache configuration, respectively. Overall, the speedups for the small workloads range from 7.8× to 23.2× for the out-of-order SuperCore and SuperCache configuration, compared to the out-of-order CryoCore and CryoCache configuration.

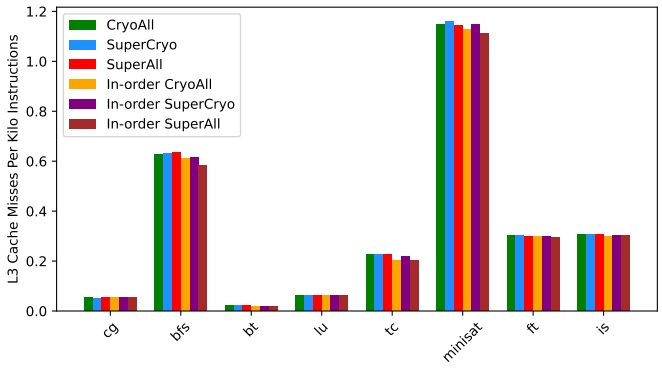
Figure 2c shows the speedup of the large workloads in various out-of-order core configurations, with respect to the out-of-order CryoCore and CryoCache configuration. The bars represent different configurations for different SPEC2006 workloads. Similar to the small workloads, if only the core is placed in the superconducting environment, the performance improvement is not substantial, with the maximum speedup being 3.9× for the `400.perlbench` workload over the baseline for an out-of-order core. Overall, the speedups for the large workloads range from 1.01× to 3.9×, barring `456.hmmer`, for the out-of-order SuperCore and CryoCache configuration, compared to the out-of-order CryoCore and CryoCache configuration. If both the core and the cache are placed in the superconducting environment, the performance improvement is more substantial for the out-of-order core. The maximum speedup for the large workloads for an out-of-order SuperCore and SuperCache configuration is 24.0× for the `456.hmmer` workload over the baseline out-of-order CryoCore and CryoCache configuration. Some workloads like `435.gromacs` and `401.bzip2` also receive speedups of more than 20× for the out-of-order SuperCore and SuperCache configuration, compared to the out-of-order CryoCore and CryoCache configuration. However, most workloads do not receive substantial speedups, with the speedup being around 1.2× and 1.7× for the out-of-order SuperCore and SuperCache configuration, compared to the out-of-order CryoCore and CryoCache configuration, respectively. Overall, the speedups for the large workloads range from 1.18× to 24.0× for the out-of-order SuperCore and SuperCache configuration, compared to the out-of-order CryoCore and CryoCache configuration.

For in-order cores, Figure 2b shows the speedup of the workloads in various in-order core configurations, with respect to the in-order CryoCore and CryoCache configuration. The bars represent different configurations for different small workloads. If only the core is placed in the superconducting environment, the performance improvement is not substantial, with the maximum speedup for the small workloads being 2.3× for the `tc` workload over the baseline for an in-order core. Overall, the speedups for the small workloads range from 1.4× to 2.3× for the in-order SuperCore and CryoCache configuration, compared to the in-order CryoCore and CryoCache configuration. If both the core and the cache are placed in the superconducting environment, the performance improvement is more substantial for both the in-order core. The maximum speedup for an in-order SuperCore and SuperCache configuration is 24.3× for the `bt` workload over the baseline in the in-order SuperCore and CryoCache configuration. Some workloads like `lu` and `cg` also receive speedups of more than 20× for the in-order SuperCore and SuperCache configuration, compared to the in-order CryoCore and CryoCache configuration. However, some workloads like `bfs` and `minisat` do not receive substantial speedups, with the speedup being around 8.4× and 9.6× for the in-order SuperCore and SuperCache configuration, compared to the in-order CryoCore and CryoCache configuration, respectively. Overall, the speedups for the small workloads range from 8.4× to 24.3× for the in-order SuperCore and SuperCache configuration, compared to the in-order CryoCore and CryoCache configuration.

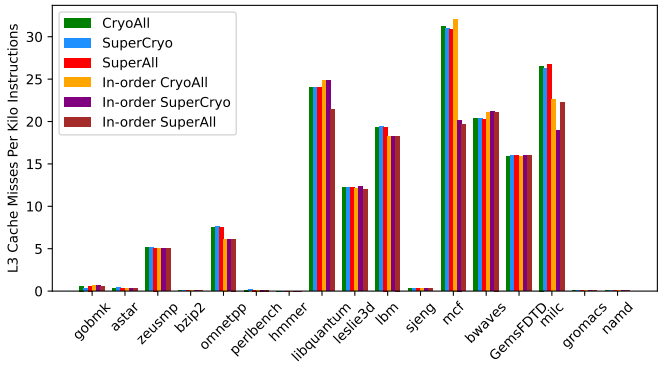
Figure 2d shows the speedup of the large workloads in various in-order core configurations, with respect to the in-order CryoCore and CryoCache configuration. The bars represent different configurations for different SPEC2006 workloads. Similar to the small workloads, if only the core is placed in the superconducting environment, the performance improvement is not substantial, with the maximum speedup being 2.6× for the `433.milc` workload over the baseline for an in-order core. Overall, the speedups for the large workloads range from 1.1× to 2.6× for the in-order SuperCore and CryoCache configuration, compared to the in-order CryoCore and CryoCache configuration. If both the core and the cache are placed in the superconducting environment, the performance improvement is more substantial for both the in-order core. The maximum speedup for the large workloads for an in-order SuperCore and SuperCache configuration is 24.5× for the `456.hmmer` workload over the baseline in the in-order SuperCore and CryoCache configuration. Some workloads like `435.gromacs`, `444.namd` and `401.bzip2` also receive speedups of more than 20× for the in-order SuperCore and SuperCache configuration, compared to the in-order CryoCore and CryoCache configuration. However, most workloads do not receive substantial speedups, with the speedup being around 1.4× and 2.6× for the in-order SuperCore and Super-

Cache configuration, compared to the in-order CryoCore and CryoCache configuration, respectively. Overall, the speedups for the large workloads range from 1.4× to 24.5× for the in-order SuperCore and SuperCache configuration, compared to the in-order CryoCore and CryoCache configuration.

Therefore, the speedups vary significantly across different workloads, with similar workloads achieving similar speedups across different core architectures. While the speedups are consistent for smaller workloads, the variation in speedup is much wider when running real-world workloads. This variation suggests that even if we could build a conventional architecture in a superconducting environment, it is unlikely to benefit general-purpose workloads uniformly. Therefore, we need to either develop a new architecture specifically optimized for superconducting environments or apply superconducting technology to specialized accelerators where there is a small amount of memory traffic instead of general-purpose compute, which could leverage the low latency and high throughput benefits of superconductors more effectively.



(a) L3 cache misses per kilo instructions (MPKI) for the small workloads.



(b) L3 cache misses per kilo instructions (MPKI) for the large workloads.

Fig. 3: L3 cache misses per kilo instructions (MPKI) for the small and large workloads.

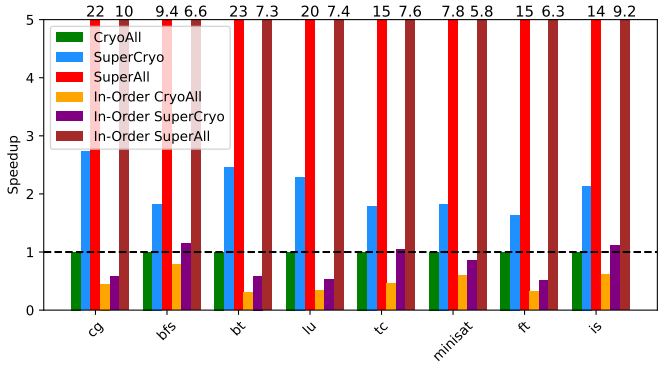
Figure 3a shows the L3 cache misses normalized to the number of instructions for the small workloads (L3 cache MPKI). The bars represent different configurations for different small workloads. Figure 3b shows the L3 cache misses normalized to the number of instructions for the large workloads (L3 cache MPKI). The bars represent different configurations for different SPEC2006 workloads. The L3 cache misses are normalized to the number of instructions to account for the different instruction counts of the workloads. We notice that the highest L3 cache MPKI for the small workloads are for workloads like `bfs` and `minisat`, which also have the lowest speedups. Similarly, the highest L3 cache MPKI for the large workloads are for workloads like `429.mcf`, `434.zeusmp`, `433.milc`, `410.bwaves` and `462.libquantum`, which also have the lowest speedups. Therefore, the L3 cache misses, and by extension the memory accesses, are a bottleneck for these workloads. On the other hand, small workloads like `lu`, `cg` and `bt`, and large workloads like `445.gobmk`, `400.perlbench`, `456.hmmer`, `444.namd`, and `473.astar` have lower normalized L3 cache misses and higher speedups, indicating that these workloads are not bottlenecked by memory accesses, and therefore, are able to achieve higher speedups.

Therefore, we conclude that the workloads which do not show substantial speedups are bottlenecked by memory accesses. This is because the memory operates at room temperature, and the core has to wait for the memory to respond to its requests, implying that the workload would not be able to achieve the speedup that the faster core could achieve. This is a potential limitation of the system, as the memory system would need to be redesigned to keep up with the faster core.

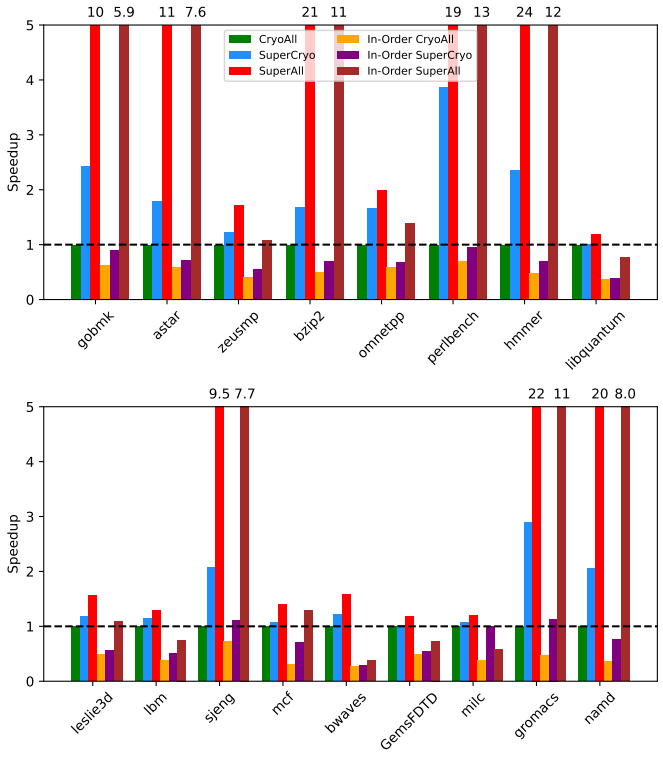
Takeaways

- The performance of workloads improved by placing components in the superconducting environment. The performance improvement was more substantial when both the core and the cache were in the superconducting environment.
- In-order cores were able to achieve a higher speedup than out-of-order cores when both the core and the cache were placed in the superconducting environment.
- The workloads that did not receive substantial speedups were bottlenecked by memory accesses. Therefore, memory systems would need to be redesigned to keep up with the faster core.
- The speedups vary significantly across different workloads, with similar workloads achieving similar speedups across different core architectures. While the speedups are consistent for smaller workloads, the variation in speedup is much wider when running real-world workloads. Therefore, we need to either develop a new architecture specifically optimized for superconducting environments or apply superconducting technology to specialized accelerators where there is a small amount of memory traffic instead of general-purpose compute.

B. Effect of Core Type (Out-of-Order vs. In-Order) on Workload Performance



(a) Speedup of small workloads with respect to the out-of-order CryoCore and CryoCache configuration, in different setups.



(b) Speedup of large workloads with respect to the out-of-order CryoCore and CryoCache configuration, in different setups.

Fig. 4: Speedup of workloads with respect to the out-of-order CryoCore and CryoCache configuration, in different setups.

We compared the speedups of various configurations of out-of-order and in-order superconducting and cryogenic cores and caches, with respect to the out-of-order CryoCore and CryoCache configuration. At a high level, we observed that the speedups are more substantial for out-of-order configurations compared to in-order configurations.

Figure 4a shows the speedup of the workloads with respect to the out-of-order CryoCore and CryoCache configuration, in different setups. The bars represent different configurations for different small workloads. Figure 4b shows the speedup of the workloads with respect to the out-of-order CryoCore and CryoCache configuration, in different setups. The bars represent different configurations for different SPEC2006 workloads. Comparing the speedups of both the out-of-order and in-order cores with respect to the out-of-order CryoCore and CryoCache configuration, we see that the speedups are more substantial for the out-of-order cores, for both the small and large workloads. The out-of-order SuperCore and CryoCache configuration performs better than or equal to both the in-order CryoCore and CryoCache configuration and the in-order SuperCore and CryoCache configuration, for both the small and large workloads.

From these figures, we can take away that for small workloads, placing components in a superconducting environment improves performance for both out-of-order and in-order cores. The performance improvement is more substantial when both the core and cache are in the superconducting environment. Interestingly, in-order cores achieve higher speedups compared to out-of-order cores when both components are superconducting. This could be because in-order cores are simpler and have less instruction-level parallelism, which could benefit from the higher clock frequency.

The out-of-order SuperCore and CryoCache configuration performs better than or equal to both the in-order CryoCore and CryoCache configuration and the in-order SuperCore and SuperCache configuration, for both the small and large workloads. Out-of-order cores can schedule instructions dynamically, which could benefit more from the higher clock frequency compared to in-order cores, which have a fixed schedule of instructions. Thus, even when all components are not superconducting, the out-of-order cores can still achieve significant performance benefits compared to in-order cores.

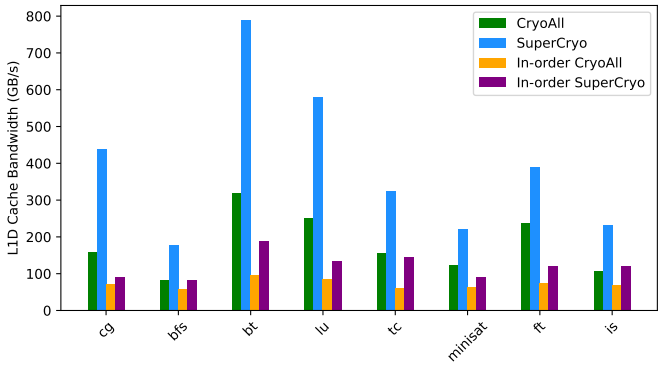
Takeaways

- The speedups are more substantial for out-of-order configurations compared to in-order configurations.
- The out-of-order SuperCore and CryoCache configuration performs better than or equal to both the in-order CryoCore and CryoCache configuration and the in-order SuperCore and CryoCache configuration, for both the small and large workloads.

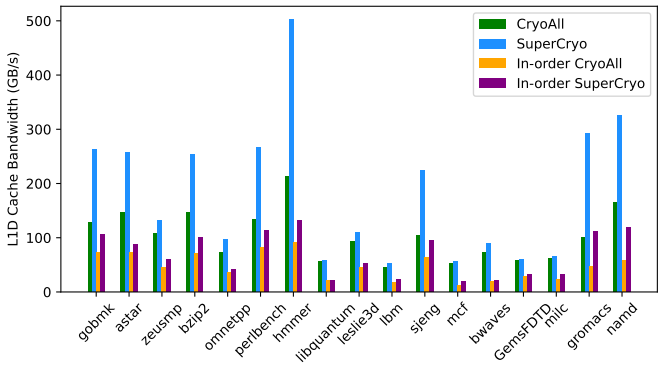
C. New Constraints for Leveraging Improved Performance from Increased Clock Frequency

In order to leverage the improved performance resulting from increased clock frequency in a superconducting environment, subsystems must meet new constraints. One such constraint is the cache bandwidth required to keep up with the faster core. We evaluated the cache bandwidths required for the L1I cache, L1D cache, L2 cache, and L3 cache for the small and large workloads.

Figure 5a shows the L1D cache bandwidth for the small workloads. The bars represent different configurations for different small workloads. Figure 5b shows the L1D cache



(a) L1D cache bandwidth for the small workloads.



(b) L1D cache bandwidth for the large workloads.

Fig. 5: L1D cache bandwidth for the small and large workloads.

bandwidth for the large workloads. The bars represent different configurations for different SPEC2006 workloads. The configurations in this figure are the CryoCore and CryoCache configuration, the SuperCore and CryoCache configuration, and their in-order variants. We chose these because they are more "realistic" than having a configuration with a superconducting cache, since memory systems for superconducting are not as scalable yet [24]. We notice that the L1D cache bandwidth is higher for the SuperCore and CryoCache configuration compared to the CryoCore and CryoCache configuration. For the small workloads, the maximum bandwidth required for the out-of-order architecture is 800 GB/s for the `bt` workload in the SuperCore and CryoCache configuration, and for in-order architecture, it is 200 GB/s for the `bt` workload in the in-order SuperCore and CryoCache configuration. For the large workloads, the maximum bandwidth required for the out-of-order architecture is 500 GB/s for the `456.hmmer` workload in the SuperCore and CryoCache configuration, and for in-order architecture, it is 130 GB/s for the `456.hmmer` workload in the in-order SuperCore and CryoCache configuration.

We observe higher L1D cache bandwidth for the SuperCore and CryoCache configuration compared to the CryoCore and CryoCache configuration, for both the small and large workloads, for both the out-of-order and in-order cores. The higher clock frequency of the core in the SuperCore configuration results in more requests to the L1D cache, which increases the number of accesses per unit time, and hence the bandwidth. The L1I caches, L2 caches, and L3 cache bandwidths are also higher for the SuperCore and CryoCache configuration compared to the CryoCore and CryoCache configuration, for both the small and large workloads, for a similar reason. For the small workloads, the maximum bandwidth required for the L1I cache is 190 GB/s for the `tc` workload in the SuperCore and CryoCache configuration; for the L2 cache, it is 390 GB/s for the `ft` workload in the SuperCore and CryoCache configuration; and for the L3 cache, it is 190 GB/s for the `cg` workload in the SuperCore and CryoCache configuration. For the large workloads, the maximum bandwidth required for the L1I cache is 130 GB/s for the `400.perlbench` workload in the SuperCore and CryoCache configuration; for the L2 cache, it is 120 GB/s for the `435.gromacs` workload in the SuperCore and CryoCache configuration; and for the L3 cache, it is 70 GB/s for the `470.lbm` workload in the SuperCore and CryoCache configuration. The workloads with the highest speedups, both in the small and large workloads, have the highest L1D cache bandwidths. If these bandwidths are not met, the speedups would not be actualized. Therefore, these high bandwidth requirements are a potential limitation of the system, and require redesigning the caches to keep up with the faster core.

Takeaways

- The workloads with the highest speedups have the highest L1D cache bandwidths.
- The overall required cache bandwidths are in the range of 130 GB/s to 800 GB/s for the small workloads and 70 GB/s to 500 GB/s for the large workloads. If these bandwidths are not met, the speedups would not be actualized.

Therefore, these high bandwidth requirements are a potential limitation of the system, and require redesigning the caches to keep up with the faster core.

V. Related Work

Cryogenic computing has been a topic of interest for researchers for a long time. Our work is based on the work of Byun et al. [1] and Min et al. [14], who have proposed a cryogenic core and a cryogenic cache, respectively. Lee et al. have also designed a cryogenic memory [25], which could be used in addition to the cryogenic core and cache to create a complete cryogenic computing system. In this work, we have adapted their designs to gem5 and conducted simulations to evaluate the performance of workloads in cryogenic computing environments.

There has been some work on superconducting computing cores as well. Ando et al. have proposed a design of an 8-bit Microprocessor based on Rapid Single Flux Quantum (RSFQ) technology, called "CORE e4" [26]. Yamanashi et al. have proposed a design of a pipelined 8-bit microprocessor

based on Single Flux Quantum (SFQ) technology, called "CORE1β" [27]. FLUX Chip by Dorojevets et al. is a chip that uses RSFQ technology [28]. It is a 16-bit microprocessor that can be clocked at 20 GHz. In this work, we just look at the high-level implication of superconducting (i.e., a clock frequency of 100 GHz) core and cache on the performance of workloads in a superconducting environment in gem5.

There has also been some work on superconducting components, part of a larger system, that may be in a room-temperature or cryogenic environment. Herr et al. have proposed a design of a 4-bit RSFQ multiplier-accumulator [29]. They ran tests on its speed and power consumption, and found that was clocked at 11 GHz and consumed 0.2 mW. Zha et al. have proposed a superconducting perceptron-based branch predictor [30]. Nagaoka et al. have proposed a design of a bit-parallel multiplier based on RSFQ technology, which can clock at 52 GHz [31]. Nagaoka et al. also proposed a design of a gate-leveled SFQ multiplier, which can clock at 48 GHz [32]. Obata et al. have proposed an SFQ integer multiplier with a systolic array architecture, clocked at 25 GHz [33]. In this work, we just look at the an entire core or cache in a superconducting environment, and its impact on the performance of workloads. We do not look at the performance of individual components, like a multiplier or a branch predictor, in a superconducting environment in gem5.

There has also been some work on temporal logic in superconducting circuits. Tzimpragos et al. [34], [35] propose that superconducting circuits can compute over temporal relationships between pulse arrivals. They propose the computational relationships between those pulse arrivals can be formalized through an extension to a temporal predicate logic. In this work, we do not look at the temporal logic in superconducting circuits, but rather the high-level implications of a superconducting core and cache on the performance of workloads in a superconducting environment in gem5.

VI. Conclusion

In this paper, we presented our methodology for conducting simulations of workloads in cryogenic computing environments using gem5. We then presented the results of our experiments and discussed their implications for the development of cryogenic computing technologies.

Our experiments show that gem5 can be used to simulate workloads in cryogenic computing environments. We used this to show that the performance of the workloads does improve with increasing CryoCore and CryoCache clock frequencies, and characterize the workloads that do not show a substantial improvement in performance. We also showed that the caches would need to be able to provide a higher bandwidth to the core to achieve the speedups shown in the experiments, and provided the bandwidths required to achieve these speedups.

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