HammerSim: A Tool to Model Rowhammer

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ABSTRACT

Recently the rowhammer vulnerability has affected modern memory devices, which allows an attacker to cause bitflips without accessing the corresponding cell. The rowhammer effects can exacerbate future memory technologies due to scaling. Hence, we need to invest in studying and mitigating rowhammer attacks. We, therefore, propose a model to simulate RowHammer in gem5 to capture the system-level interaction of RowHammer.

1 INTRODUCTION

Dynamic random access memory, or DRAM, is the *de-facto* choice for main memory design due to its cost-effectiveness. However, due to scaling, researchers have noticed variations in the nominal parameters of these devices [6, 18, 32]. Recently, it has been found that accessing (or `ACT`ivating) a particular cell of a DRAM module repeatedly causes data corruption in the neighborhood. This is called RowHammer [4, 15]. There have been extensive studies done to study and mitigate rowhammer [2, 15, 17, 25, 29]. Most of such variations or data corruptions are unfortunately not captured in simulators [8].

We aim at closing the gap between DRAM DIMMs and its simulated counterpart along the lines of RowHammer. Researchers have characterized bitflips in the past [1, 23, 24, 30]. There exists circuit-level models to simulate RowHammer [13]. FPGAs help in studying RowHammer with software-based memory controllers [11, 21]. However, this approach necessitates specialized setup. Currently we do not posses a comprehensive model of RowHammer at the system level. Developing such a model is crucial as this enables us to study the interaction of workloads and data-corruption alongside estimating the behavior of future DRAM technology.

As a precursor to the simulation model of RowHammer, we performed extensive hammering on different DRAM modules (or DIMMs[1]). The analytical model of RowHammer that people reply on assumes an equally likely probability of a bitflip in a DRAM row when the number of accesses crosses a certain threshold in the neighborhood [2, 15, 17, 25, 29]. We saw that this is not the case on actual DRAM DIMMs. Most unique bitflips saturate over time as not all regions of the memory are vulnerable. This is shown in Figure 1, where we see that the number of unique bitflips saturates over time. This information is not previously captured while modeling RowHammer, which can largely influence the future designs of mitigation techniques.

Modeling the aforementioned reliability would enable researchers to estimate the probability of obtaining the correct output of a program in a non-trusted environment like the cloud. The RowHammer threshold is decreasing as DRAMs are becoming denser [14], which motivates the need for such a model. In this abstract, we propose a system-level RowHammer model called *HammerSim*, which we have integrated with gem5 [19].

[1]A DIMM refers to dual inline memory module.

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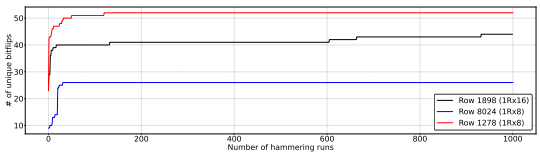


Figure 1: Count of unique bitflips on different DRAM DIMMs' row.

2 METHODOLOGY

Our objective is to model RowHammer closely to its hardware counterpart. Toward this, we have attempted to reproduce bitflips on real DDR4 DIMMs. Based on our findings and previous literature, we conclude that RowHammer is a result of a combination of several probability distributions. These distributions are primarily based on the inherent variations induced during manufacturing time [15, 23, 31]. However, there is no deterministic correlation between process variation and RowHammer [15]. We observed that a weak memory cell (or a capacitor) may or may not exhibit a bitflip under a RowHammer attack. This adds to the randomness of RowHammer. This is a consistent observation across several attack papers, where at each hammering instance, a vulnerable bit does not always flip [7, 12, 23, 27, 28, 31]. Figure 2 shows instances of bitflips on a single row (1278), across 4 different runs. A white dot represents a bitflip in a column. Figure 2(f) plots the histogram of bitflip count across 1000 hammering instances.

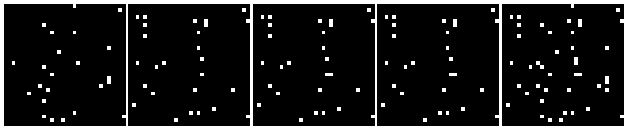
2.1 Simulation Model

Overall, we have the following probabily distributions for modelling rowhammer bitflips:

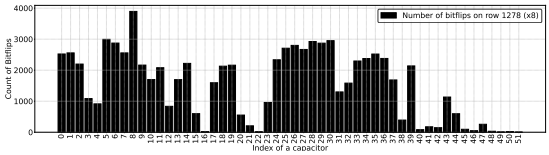
2.1.1 A model for process variaiton. We model a variation map based on VARIUS [26], a statistical model of process variation. It models process variation as a multivariate normal distribution. The outcome is a binary decision: *whether a given cell or a capacitor is weak or a strong cell?* This is represented as `WC`, or weak cell in Equation 1.

2.1.2 Uniform probability for flipping a bit. For a given *weak* cell `WC`, we use a uniform probability function to flip the cell. This is a property of the DIMM. We experimentally determine the probability which ranges from $\frac{1}{5\times10^{10}}$ to $\frac{1}{5\times10^{8}}$ for a bitflip. This can be tuned by the user in the simulation framework. `F_WC` represents a *flippable* bit in Equation 1

2.1.3 Probability escalation of an N-sided rowhammer attack. This probability distribution is correlated with the other aggressor rows in the neighborhood. For this, we use counter-pairs while counting

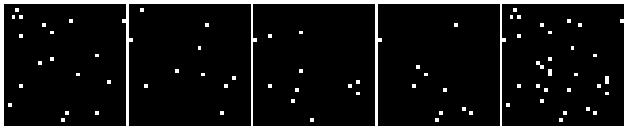


(a) Run 1 (b) Run 2 (c) Run 3 (d) Run 4 (e) Superimposed Image

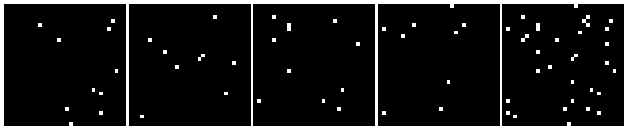


(f) Histogram of bitflip counts on row number 1278 across 1000 runs.

Figure 2: Observed bitflips on a single row on a width 8 DRAM DIMM.



(a) Run 1 (b) Run 2 (c) Run 3 (d) Run 4 (e) Superimposed Image



(f) Run 1 (g) Run 2 (h) Run 3 (i) Run 4 (j) Superimposed Image

Figure 3: Simulated result of bitflips on a single row. The top set of runs used the variation map taken from the actual DRAM DIMMs. The bottom set is generated using a statistical model of process variation.

`ACTs`. This is also a property of the DIMM. We use an experimentally determined probability of $\frac{1}{2.5\times10^3}$ for the same.

2.1.4 Half-double. Half-double [9, 16] can only be modeled via counters of triggering a bitflip. For every `ACT` on a row, we have to maintain counters for each of the rows (4) in the blast radius. This is not trivial to maintain as checking the memory after each `ACT` increase the simulation time exponentially. Therefore, we simply monitor half-double access patterns only during a refresh event.

We combine these aforementioned probability distributions in a conventional manner, which is given by:

$$P_{bitflip} = P(WC|F\_WC) \times \frac{1}{P(n\text{-}sided)} \times \frac{1}{P(half\text{-}double)} \quad (1)$$

3 ANALYSIS

HammerSim is implemented on gem5 [19], a full-system cycle-level simulator. We modeled the probability distributions of RowHammer (referred to in Section 2) within gem5's memory interface. In addition, we have also modeled the mitigation mechanism installed on one of the DRAM vendors using the reverse-engineered understanding of the same depicted in U-TRR [10][2]. The RowHammer bitflip map generated via gem5 is shown in Figure 3. Figures 3(a)–3(e) simulate bitflips in gem5 with a variation map taken from the actual DRAM DIMM. The measured similarity index between the real and the simulated run is 0.31 in terms of JS Divergence [22] value (lower is better). The lower set of images represents bitflips with a statistically generated variation map.

This abstract does a general analysis of RowHammer consequences on HPC workloads taken from GAPBS [5] and NAS-Parallel benchmark suite [3]. We simulate an x86 system with 2 levels of caches (L1: 32KB + 32KB; L2: 256KB). Figure 4 shows the instances of row `ACTs` crossing the LPDDRx (16.8K – 4.8K), DDR4 (45K) and DDR3 (139K) thresholds. We see that there are 20041.16 instances on average, where rows cross the DDR4 threshold of 45K ACTs. The figure is worse for LPDDR [20] DIMMs, where the threshold count is even lower. The threshold is likely to be even lower for DDR5 DRAM DIMMs.

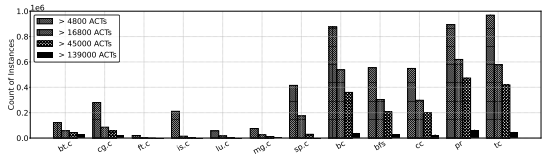


Figure 4: Observed instances of `ACT` count crossing 4.8K, 16.8K (LPDDRx), 45K (DDR4) and 139K (DDR3).

We did a bitflip estimation of RowHammer by probabilistically flipping bits during runtime. We tuned the probability of a bitflip from $\frac{1}{10^9}$ to 1 for each of these benchmarks. Figure 5 plots the same. This shows that even benign applications have a significant probability of flipping bits. Note that for this experiment, we have only considered N-sided probability. This value is predicted to worsen due to increasing density.

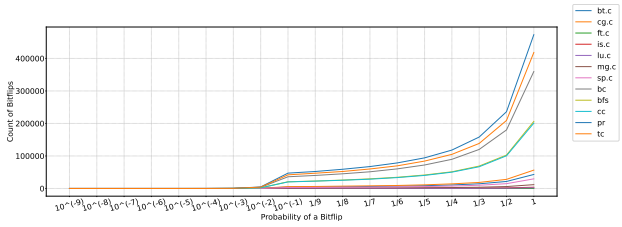


Figure 5: Estimation of bitflips by varying the probability of a bitflip.

4 CONCLUSION

In this abstract, we have proposed a preliminary model of RowHammer. The model is presented as a tool called HammerSim, which is

[2]correspond's to U-TRR's Vendor B.

implemented in a full-system simulator. This allows us to study the interaction between data-corruption and real-world workloads. In the future, we plan on quantitatively evaluating RowHammer and its mitigation as a metric at the system-level using HammerSim. Furthermore, we plan on extending this infrastructure to simulate cloud environments with malicious programs running alongside benign applications to create a more realistic scenario.

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